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From:	**Elizabeth A. Stanek**
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Attorney Docket No. 5649-927DV PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Hyoung-Joon Kim et al. Confirmation No.: 7889
Serial No.: 10/706,647 Group Art No.: 2822
Filed: November 12, 2003 Examiner: Toniae M. Thomas
For: METHODS OF FABRICATING INTEGRATED CIRCUIT DEVICES PROVIDING IMPROVED SHORT PREVENTION

March 30, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INTERVIEW SUMMARY

Applicants concur with the Interview Summary provided by the Examiner. In particular, on February 2, 2005, Applicants' representative, Elizabeth A. Stanek, was contacted by Examiner Thomas regarding a proposed Examiner's Amendment to place the claims in the present application in condition for allowance. During the interview, Applicants' representative and the Examiner discussed Independent Claims 1, 5 and 9 and reached agreement that the claims should be amended as follows:

1. A method of fabricating an integrated circuit device comprising:
forming a conductive layer on a microelectronic substrate;
forming a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;
forming a second insulating layer on the microelectronic substrate to cover the first insulating layer; and
etching the second insulting layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate, such that a portion of the second insulating layer remains on an upper surface of the first insulating layer.

5. A method of fabricating a self-aligned contact structure for a microelectronic device, the method comprising:
forming a conductive layer on a microelectronic substrate;
forming a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;
forming a second insulating layer on the microelectronic substrate to cover the first insulating layer;
etching the second insulating layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate, such that a portion of the second insulating layer remains on an upper surface of the first insulating layer; and

forming a conductive region disposed laterally adjacent to the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region.

9. A method of fabricating an integrated circuit memory device, comprising:
forming a first bit line comprising:
forming a first conductive layer on a microelectronic substrate; and
forming a first insulating layer on the first conductive layer, the first insulating layer including a first overhanging portion that extends beyond the first conductive layer; and
forming a second bit line comprising:
forming a second conductive layer on the microelectronic substrate; and
forming a second insulating layer on the second conductive layer, the second insulating layer including a second overhanging portion that extends beyond the second conductive layer;
forming a third insulating layer on the microelectronic substrate to cover the first and second bit lines; and
etching the third insulating layer to simultaneously form a first sidewall insulating layer region disposed laterally adjacent to a first sidewall of the first conductive layer, and a second sidewall insulating region disposed laterally adjacent to a second sidewall of the second conductive layer, wherein the first sidewall insulating region extends between the first overhanging portion of the first insulating layer and the microelectronic substrate, and the second sidewall insulating region extends between the second overhanging portion of the second insulating layer and the microelectronic substrate, such that a portion of the third insulating layer remains on an upper surface of the first insulating layer and an upper surface of the second insulating layer.

Applicants' representative and the Examiner reached agreement that the above claims recite patentable subject matter and would place the case in condition for allowance. Accordingly, Applicants' representative authorized the Examiner to enter an Examiner's Amendment amending the claims, as shown above, thereby placing the case in condition for allowance.

Respectfully submitted,

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I hereby certify that this correspondence is being sent by facsimile transmission to Commissioner for Patents, Alexandria, VA 22313-1450, at (703) 872-9306 on March 30, 2005.

Erin A. Campion